a first plurality of metal floods connected to the respective plated holes to form a plurality first plates, the first metal floods on the first plane;

a second signal path on the second plane; and

a second plurality metal floods connected to the second signal path to form a plurality of second plates above the respective first plates, the second plate on the second plane.

2. (Previously Amended) The apparatus of claim 1 wherein each set of first and second plates form a capacitance.

3. (Cancelled)

4. (Cancelled)

5. (Previously Amended) The apparatus of claim 1 wherein the first and second signal paths are adjacent to each other.

6. (Previously Amended) The apparatus of claim 1 wherein the first plane is a ground plane or a power plane.

7. (Previously Amended) The apparatus of claim 6 wherein each of the first metal floods is an isolated area in the first plane.

8. (Currently Amended) A method comprising:

providing a dielectric material having a first plane and a second plane opposite the first plane;

connecting a first signal path to said first plane via a plurality of plated holes formed through the dielectric material at different locations along said first signal path, the first signal path on said second plane;

forming a plurality of first plates by connecting a plurality of first metal floods to the respective plated holes, the first metal floods on the first plane; and

connecting a plurality of second metal flood to a second signal path on the second plane to form a plurality of second plates above the respective first plates.

9. (Original) The method of claim 8 wherein the first and second plates form a capacitance.

10. (Cancelled)

11. (Cancelled)

12. (Previously Amended) The method of claim 8 wherein the first and second signal paths are adjacent to each other.

13. (Previously Amended) The method of claim 8 wherein the first plane is a ground plane or a power plane.

14. (Previously Amended) The method of claim 13 wherein each of the first metal floods is an isolated area in the first plane.

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Cancelled)

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Currently Amended) The apparatus of claim 2 further comprising a second dielectric material disposed on said first plane of said dielectric material and a third dielectric disposed on said second plane of said dielectric material, wherein the capacitance is a buried intersignal capacitance.

24. (Cancelled)

25. (Currently Amended) The method of claim 9 forming a second dielectric material on said first plane of said dielectric material, and forming a third dielectric material on said second plane of said dielectric material, wherein the capacitance is a buried intersignal capacitance.

26. (Cancelled)

27. (Cancelled)

28. (Previously Amended) An apparatus comprising:

a printed circuit board;

a first transmission line on a first layer of the printed circuit board;

a second transmission line on the first layer of the printed circuit board; and

a plurality of capacitors connected to the first transmission line and the second transmission line at different locations, each of the capacitor comprising:

a first plate connected to the first transmission line by a plated hole, the first plate on a second layer of the printed circuit board;

a second plate connected to the second transmission line, the second plate on the first layer of the printed circuit board; and

a dielectric layer between the first plate and the second plate, the dielectric layer between the first layer of the printed circuit board and the second layer of the printed circuit board.

29. (Previously Added) The apparatus of claim 28 wherein the first plate is above the second plate.

30. (Previously Added) The apparatus of claim 28 wherein the second plate is above the first plate.

31. (Previously Added) The apparatus of claim 28 wherein the capacitor is a buried intersignal capacitor.

32. (Previously Added) The apparatus of claim 31 wherein the buried intersignal capacitor mode compensates to improve signal quality in the printed circuit board.

33. (Previously Added) The apparatus of claim 32 wherein the buried intersignal capacitor matches the propagation speed of odd-mode switch signals with the propagation speed of even-mode switch signals.

34. (Cancelled)

35. (Cancelled)

36. (Cancelled)

37. (Previously Added) The apparatus of claim 28 wherein the first transmission line is adjacent to the second transmission line.

38. (Previously Added) The apparatus of claim 28 wherein the first transmission line is inductively coupled to the second transmission line.

39. (Previously Added) The apparatus of claim 28 wherein the first transmission line and/or second transmission line are routed as microstrips.

40. (Previously Added) The apparatus of claim 28 wherein first transmission line and the second transmission line are routed on surface layers of the printed circuit board.